

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 Claim 1 (currently amended): An apparatus for performing low  
2 density parity check encoding operations, the apparatus  
3 comprising:  
4           memory including a set of memory locations for storing  
5 ~~L sets of~~ Z-bit vectors, where Z is a positive integer greater  
6 than one and L is a positive integer;  
7           a vector unit operation processor including a circuit  
8 for performing Z parity calculations in parallel to compute a Z-  
9 bit vector, each bit of the computed Z-bit vector being  
10 generated by one of the Z parity calculations, an accumulator  
11 for storing the computed Z-bit vector, and an output device for  
12 passing the computed Z-bit vector to the said memory ~~in response~~  
13 ~~to operation instructions;~~ and  
14           a ~~switching~~ reordering device coupled to the memory  
15 and to the vector unit operation processor, the ~~switching~~  
16 reordering device for passing a Z-bit vectors ~~vector~~ between  
17 said memory and said vector unit operation processor and for  
18 performing a bit level reordering operation on elements of at  
19 least one Z-bit vector, in response to ~~switch~~ reordering control  
20 information, as the at least one Z-bit vector is passed between  
21 said memory and said vector unit operation processor by said  
22 reordering device.

1 Claim 2 (original): The apparatus of claim 1, further  
2 comprising:  
3           an ordering control module coupled to said memory for  
4 generating read and write indices; and  
5           an operation control module coupled to said vector  
6 unit operation processor for generating unit operation  
7 instructions.

1 Claim 3 (currently amended): The apparatus of claim 2, wherein  
2 the ordering control module is further coupled to said  
3 reordering ~~switch~~ device for generating said reordering ~~switch~~

4 control information used to control the ~~switching of~~ reordering  
5 for said at least one Z-bit vector.

1 Claim 4 (currently amended): The apparatus of claim 1, wherein  
2 the ~~switching~~ reordering device includes circuitry for  
3 performing a vector ~~rotation~~ element reordering operation that  
4 includes a bitwise rotation operation to generate a reordered  
5 rotated Z-bit vector.

1 Claim 5 (currently amended): The apparatus of claim 2, wherein  
2 the ordering control module stores information on the order of  
3 the Z-bit vectors are to be read out of the memory and  
4 information on the order of the Z-bit vectors are to be written  
5 into the memory.

1 Claim 6 (currently amended): The apparatus of claim 5, 2,  
2 wherein the ordering control module further stores bitwise  
3 rotation operation information ~~on the rotation~~ to be used in  
4 generating said re-ordering control information performed on the  
5 ~~read-out vectors from said memory by said switch.~~

1 Claim 7 (original): The apparatus of claim 2, wherein the  
2 ordering control module sequentially generates index  
3 identifiers, each identifier controlling the memory to access  
4 memory locations corresponding to a vector as part of a single  
5 SIMD instruction.

1 Claim 8 (original): The apparatus of claim 7, wherein each  
2 identifier is a single memory address.

1 Claim 9 (original): The apparatus of claim 2, wherein said  
2 operation control module stores operation instructions, each  
3 instruction controlling the operation at said vector unit  
4 operation processor.

1 Claim 10 (original): The apparatus of claim 9, wherein the  
2 operation control module sequentially generates operation

3 instructions, each instruction controlling said vector unit  
4 operation processor to perform instructed operations.

1 Claim 11 (currently amended): The apparatus of claim 4, ~~further~~  
2 further comprising an encoder control module coupled to said  
3 ordering control module, the encoder control module including  
4 means for supplying information to said ordering control module  
5 used to control the order in which each of the L Z-bit vectors  
6 is to be read out of said memory, their associated reorderings  
7 ~~rotations~~, and the order to be written into said memory.

1 Claim 12 (currently amended): The apparatus of claim 11,  
2 wherein the encoder control module ~~device~~ is further coupled to  
3 said operation control module, the encoder control device  
4 including means for supplying information to said operation  
5 control module used to generate operation instructions.

1 Claim 13 (currently amended): A method of performing low  
2 density parity check encoding operations, the method comprising:

3 storing L ~~sets of~~ Z-bit vectors in a memory device,  
4 where Z is a positive integer greater than one and L is a  
5 positive integer;

6 reading one of said ~~sets of~~ Z-bit L stored Z-bit  
7 vectors from said memory device ~~stored L sets of Z-bit vectors~~;

8 ~~rotating~~ performing a bit level reordering of the bits  
9 in said read one of said ~~Z-bit~~ Z-bit vectors; and

10 operating a vector unit processor to perform a  
11 plurality of parity check combining operations in parallel to  
12 combine the bits of the ~~rotated~~ reordered Z-bit Z-bit vector  
13 with a Z-bit vector stored in said vector unit processor to  
14 generate a new Z-bit vector.

1 Claim 14 (currently amended): The method of claim 13, further  
2 comprising:

3 storing said new ~~Z-bit~~ Z-bit vector in said memory device  
4 in the place of one of the L stored ~~L-sets of Z-bit~~ Z-bit  
5 vectors.

1 Claim 15 (currently amended): The method of claim 14, wherein  
2 said parity check combining operations performed by said vector  
3 unit processor are exclusive OR operations.

1 Claim 16 (currently amended): ~~The method of claim 15~~ A method  
2 of performing encoding operations, the method comprising:  
3 storing L Z-bit vectors in a memory device, where Z is  
4 a positive integer greater than one and L is a positive integer;  
5 reading one of said L stored Z-bit vectors from said  
6 memory device;  
7 reordering the bits in said read one of said Z-bit  
8 vectors; and  
9 operating a vector unit processor to perform a  
10 plurality of combining operations to combine the bits of the  
11 reordered Z-bit vector with a Z-bit vector stored in said vector  
12 unit processor to generate a new Z-bit vector  
13 storing said new Z-bit vector in said memory device in the  
14 place of one of the L stored Z-bit vectors  
15 wherein said combining operations performed by said vector  
16 unit processor are exclusive OR operations; and  
17 wherein said encoding method is a low density parity check  
18 encoding method.

1 Claim 17 (currently amended): The method of claim 14, further  
2 comprising:

3 executing a set of stored machine executable  
4 instructions to control the ~~rotation~~ reordering of the read Z  
5 bit vector, said reordering including a rotation operation.

1 Claim 18 (currently amended): The method of claim 14, further  
2 comprising:

3 using the executed set of stored machine executable  
4 instructions to determine which one of said L ~~sets of~~ stored ~~Z~~  
5 ~~bit~~ Z-bit vectors is to be read from memory.

1 Claim 19 (currently amended): The method of claim 14, further  
2 comprising:

3 using the executed set of stored machine executable  
4 instructions to determine when one of said ~~sets of~~ L stored ~~Z~~  
5 ~~bit~~ Z-bit vectors is to be read from memory.

1 Claim 20 (currently amended): The method of claim 19, further  
2 comprising:

3 using the executed set of stored machine executable  
4 instructions to determine which one of the L stored ~~L-sets of Z~~  
5 ~~bit~~ Z-bit vectors is to be replaced by storing the new ~~Z-bit~~ Z-  
6 bit vector in said memory device.

1 Claim 21 (currently amended): The method of claim 19, further  
2 comprising:

3 resetting the ~~Z-bit~~ Z-bit vector stored in said vector unit  
4 processor at the same time said new ~~Z-bit~~ Z-bit vector is  
5 stored.

1 Claim 22 (currently amended): The method of claim 14, further  
2 comprising:

3 resetting the ~~Z-bit~~ Z-bit vector stored in said vector unit  
4 processor at the same time said new ~~Z-bit~~ Z-bit vector is  
5 stored.

1 Claim 23 (currently amended): The method of claim 14, further  
2 comprising:

3 using the executed set of stored machine executable  
4 instructions to determine which one of the L stored ~~L-sets of Z~~  
5 ~~bit~~ Z-bit vectors is to be replaced by storing the new ~~Z-bit~~ Z-  
6 bit vector in said memory device.

1 Claim 24 (currently amended): A method of performing low  
2 density parity check encoding operations, the method comprising:  
3 storing ~~L sets of~~ Z-bit vectors in a memory device,  
4 where Z is a positive integer greater than one and L is a  
5 positive integer;

6 reading one of said ~~sets of~~ Z bit vectors from said  
7 stored L sets of ~~Z-bit~~ Z-bit vectors;

8 operating a vector unit processor to perform a  
9 plurality of parity check combining operations in parallel to  
10 combine the bits of the ~~rotated Z-bit~~ read Z-bit vector with a  
11 Z-bit vector stored in said vector unit processor to generate a  
12 new Z-bit vector;

13 ~~rotating~~ reordering the bits in said new ~~Z-bit~~ Z-bit  
14 vector by performing a bit level reordering of bits in the new  
15 Z-bit vector to produce a reordered Z-bit vector; and

16 storing said reordered ~~rotated new Z-bit~~ Z-bit vector  
17 in said memory device in the place of one of the L stored ~~L-sets~~  
18 ~~of Z-bit~~ Z-bit vectors.

1 Claim 25 (currently amended): ~~The method of claim 24, A method~~  
2 of performing encoding operations, the method comprising:

3 storing L Z-bit vectors in a memory device, where Z is  
4 a positive integer greater than one and L is a positive integer;

5 reading one of said Z-bit vectors from said L stored  
6 Z-bit vectors;

7 operating a vector unit processor to perform a  
8 plurality of combining operations to combine the bits of the  
9 read Z-bit vector with a Z-bit vector stored in said vector unit  
10 processor to generate a new Z-bit vector;

11 reordering the bits in said new Z-bit vector by cyclicly  
12 shifting the position of bits in the new Z-bit vector to  
13 implement a cyclic shift operation that produces a reordered Z-  
14 bit vector; and

15 storing said reordered Z-bit vector in said memory  
16 device in the place of one of the L stored Z-bit vectors;

17 wherein said combining operations performed by said vector  
18 unit processor are exclusive OR operations; and  
19 wherein said encoding method is a low density parity check  
20 encoding method.

1 Claim 26 (currently amended): The method of claim 25, further  
2 comprising:

3 executing a set of stored machine executable  
4 instructions to control the reordering ~~rotation~~ of the read Z  
5 ~~bit~~ Z-bit vector and to determine which one of the L stored Z  
6 ~~sets of Z-bit~~ Z-bit vectors is to be replaced by storing said  
7 ~~rotated new Z-bit~~ reordered Z-bit vector in said memory device.

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**